

Substitute for form 1449A/PTO

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Sheet	1	of	2
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Complete if Known

Application Number	TO BE ASSIGNED
Filing Date	September 22, 2003
First Named Inventor	Priyadarsan Patra et al.
Group Art Unit	2825 (Anticipated)
Examiner Name	Annette M. Thompson (Anticipated)
Attorney Docket Number	2207/1254202

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O. Chirang

Date Considered

1/17/06

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Substitute for form 1449A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	TO BE ASSIGNED
		Filing Date	September 22, 2003
		First Named Inventor	Priyadarsan Patra et al.
		Group Art Unit	2825
		Examiner Name	Annette M. Thompson (Anticipated)
Sheet 2 of 2	Attorney Docket Number	2207/1254202	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
TD	1	TILOS: A Posynomial Programming Approach to Transistor Sizing. FISHBURN, J.P., DUNLOP, A.E. Available from IEEE Service Cent. (Cat. Publ. by IEEE, New York, NY, USA, N 85CH2233-5), Piscataway, NJ, USA p. 328-328.	
TD	2	Timing driven cell replication during placement for cycle time optimization. NEUMANN, Ingmar and POST, Hans-Ulrich. Integration-The VLSA Journal 27 (1999) pp. 131-141.	
TD	3	Gate Size Optimization for Row-based Layouts, MAHESHWARI, Naresh and SAPATNEKAR, Sachin S.; Midwest Symposium on Circuits and Systems, Vol. 2 (1995). IEEE, Piscataway, NJ, USA 95CB35853, pp. 777-780.	
TD	4	Automatic transistor sizing in high performance CMOS logic circuits. HOPPE, B; NEUENDORF, G; and SCHMIDT-Landsiedel D.; VLSI and Computer Peripherals. Available from IEEE Service Cent. (Cat. Publ. by IEEE, IEEE Service Center, Piscataway, NJ, USA., Catalog No. 89CH2704-5), Piscataway, NJ, USA, pp. 5/25-27.	
TD	5	Timing optimization of mixed static and domino logic. ZHAO, Min, SAPATNEKAR, Sachin S. Proceedings - IEEE International Symposium on Circuits and Systems. v. 6 1998. IEEE, Piscataway, NJ, USA, 98CH36187, pp. 266-269.	
TD	6	Interleaving Buffer Insertion and Transistor Sizing into a Single Optimization. JIANG, Yanbin; SAPATNEKAR, Sachin S.; BAMJIL, Cyrus; and KIM, Juho; Available from IEEE Service Cent (Cat. Publ by IEEE, New York, NY, USA, 1063-8210/98), Piscataway, NJ, USA, pp. 625-633.	
TD	7	MOSIZ: A Two-step Transistor Sizing Algorithm based on Optimal Timing Assignment Method for Multi-stage Complex Gates. DAI, Zhi-jian and ASADA, Kunihiro; Available from IEEE Service Cent. (Cat. Publ. by IEEE, New York, NY, USA, CH2671-6/89/0000-0201), Piscataway, NJ, USA, pp. 17.3.1-17.3.4.	
TD	8	ICOACH: A circuit optimization aid for CMOS high-performance circuits. CHEN, H.Y. and KANG, S.M. Available from Elsevier INTEGRATION, the VLSI journal 10 (1991) 185-212.	

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